Massachusetts Institute of Technology

Nanoelectronics Laboratory

Jeehwan Kim

Assistant Professor

Mechanical Engineering

Materials Science and Engineering

Research Laboratory of Electronics

1. Extremely cost-effective semiconductor layer-transfer
: Graphene-based layer transfer (GBLT)

2. Highly uniform advanced RRAM
: Epitaxial RAM (ERAM)

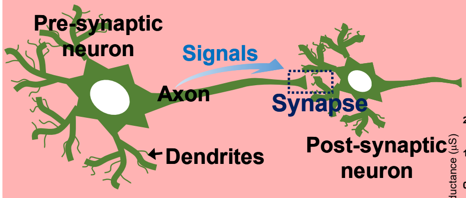
Nanoelectronics Lab

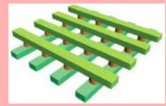
Advanced Electronics/ Computing

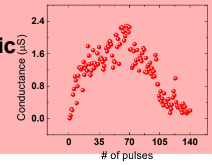
Process Innovation

Novel material development

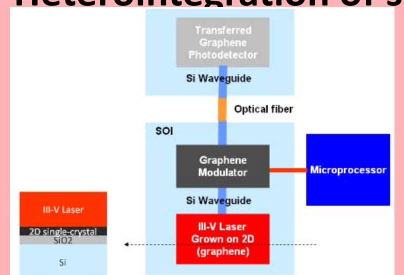
Neuromorphic computing for AI

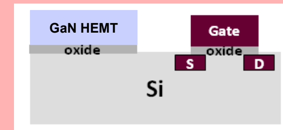




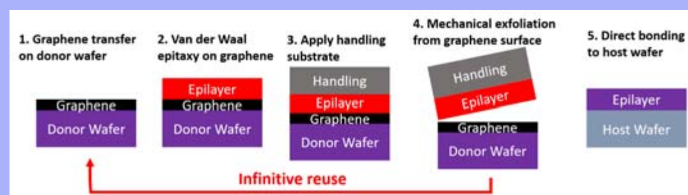


Heterointegration of semiconductors



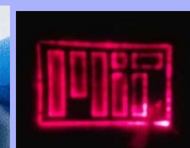


Graphene-based layer transfer

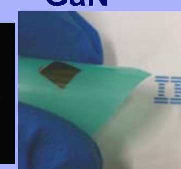


Advanced photovoltaics/LEDs

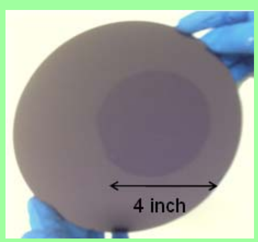
GaAs

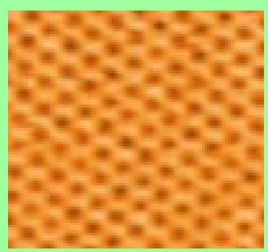


GaN

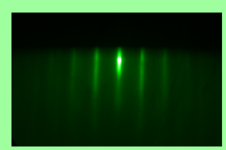


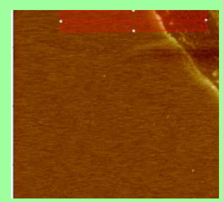
Wafer-scale single-crystalline graphene

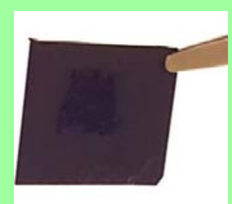




Wafer-scale single-crystalline 2D materials (TMDCs)



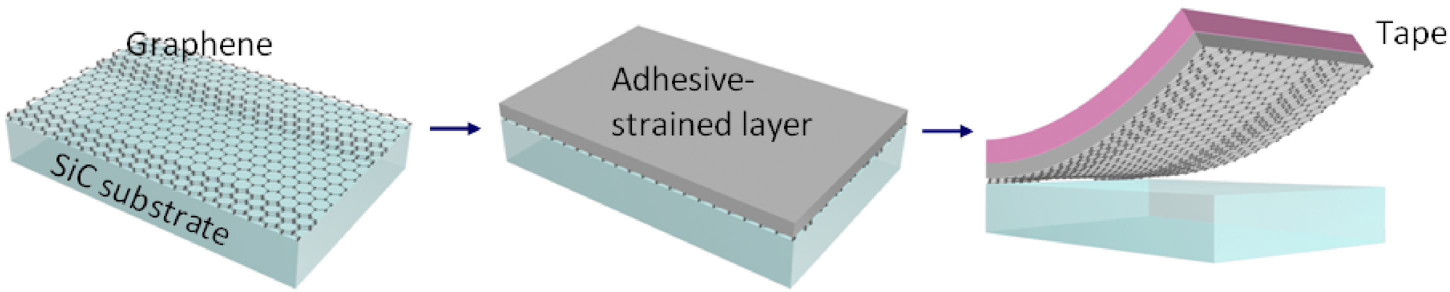




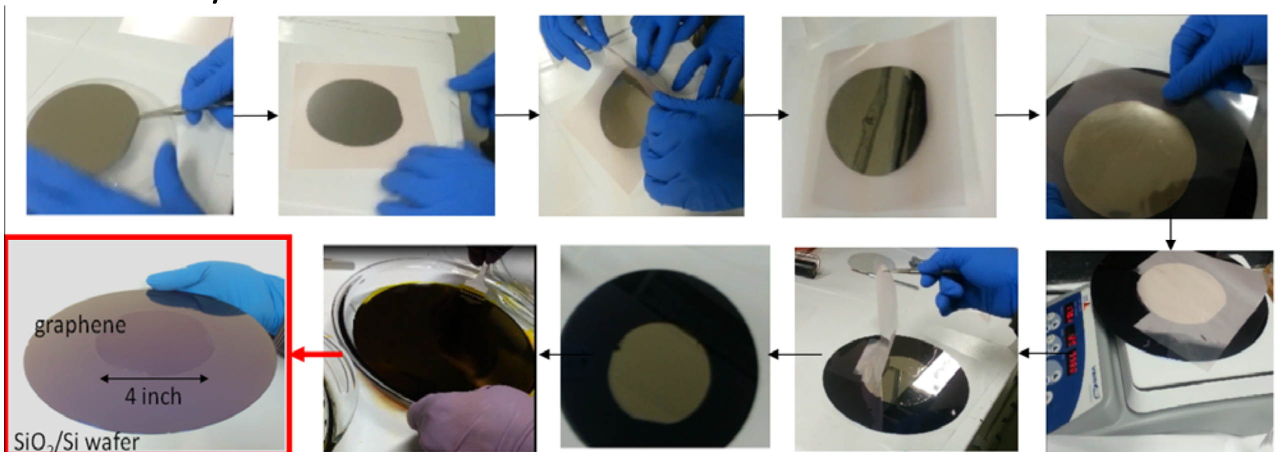
Wafer-scale single-crystalline graphene

1 ML graphene growth on SiC

Mechanical exfoliation

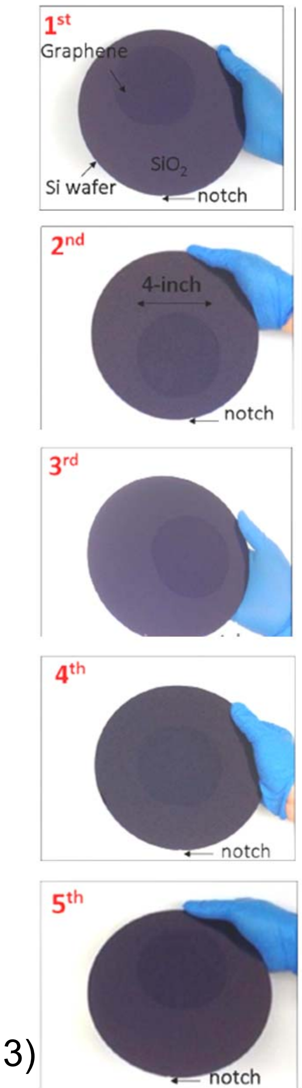


Exfoliation/transfer



99% Yield

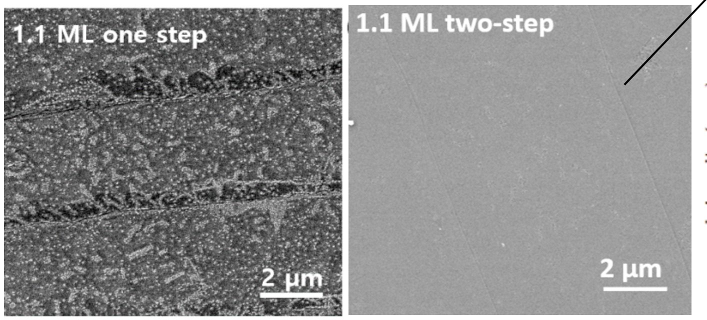
From one SiC substrate



J. Kim et al., ***Science***, Vol. 342, 833 (2013)
S. Bae**, J. Kim** et al., ***PNAS***, Under review

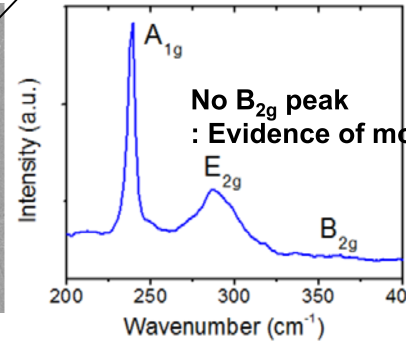
World first single-crystalline monolayer TMDC

Perfectly monolayer

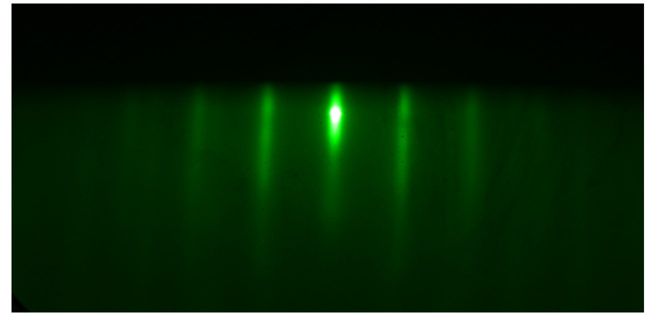


Our new growth method

Raman spectra

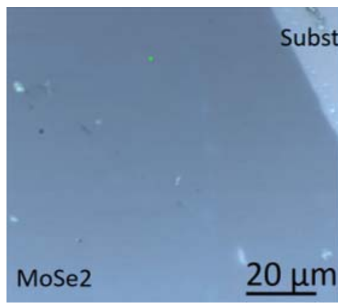


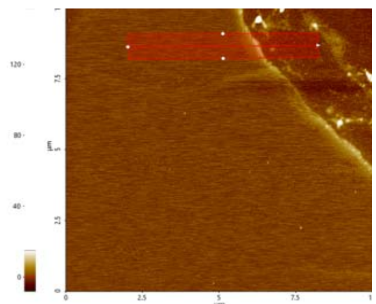
Single-crystalline (RHEED)



Six fold symmetry

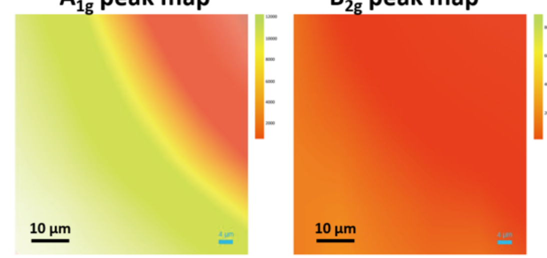
High yield wafer-scale transfer / perfectly monolayer



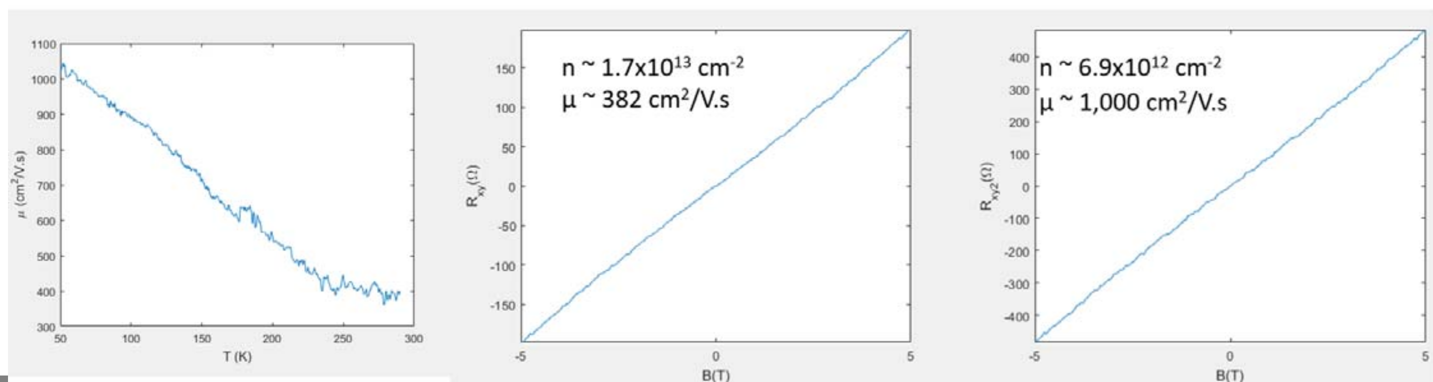


A_{1g} peak map

B_{2g} peak map



Highest electron mobility for grown $MoSe_2$: 400 cm^2/V-s at R.T/1000 cm^2/V-s at L.T



1. Extremely cost-effective semiconductor layer-transfer
   : Graphene-based layer transfer (GBLT)

2. Highly uniform advanced RRAM
   : Epitaxial RAM (ERAM)

Massachusetts Institute of Technology

Extremely cost-effective semiconductor layer-transfer

: Graphene-based layer transfer (GBLT)

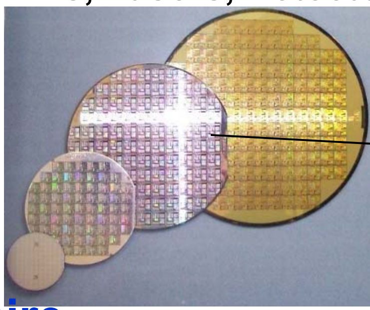
Jeehwan Kim
Research Group
http://jeehwanlab.mit.edu

Major bottleneck for advancing semiconductor technology

Substrate: Essential building block to form Electronic/optoelectronic devices

Epitaxial growth: Process for forming device film structures on the substrate

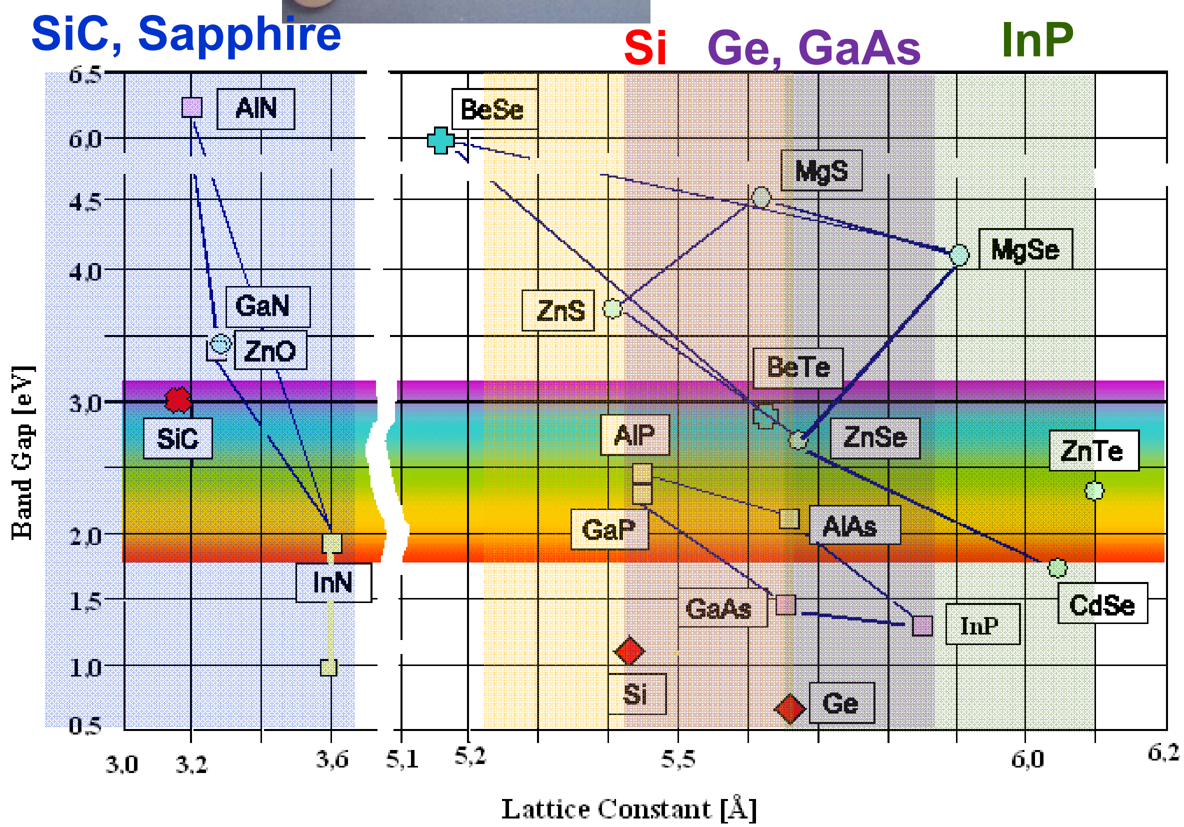
FETs, LEDs, Lasers, Detectors



Epitaxy of single-crystalline films is required on given available substrates

Epitaxial films

Substrate



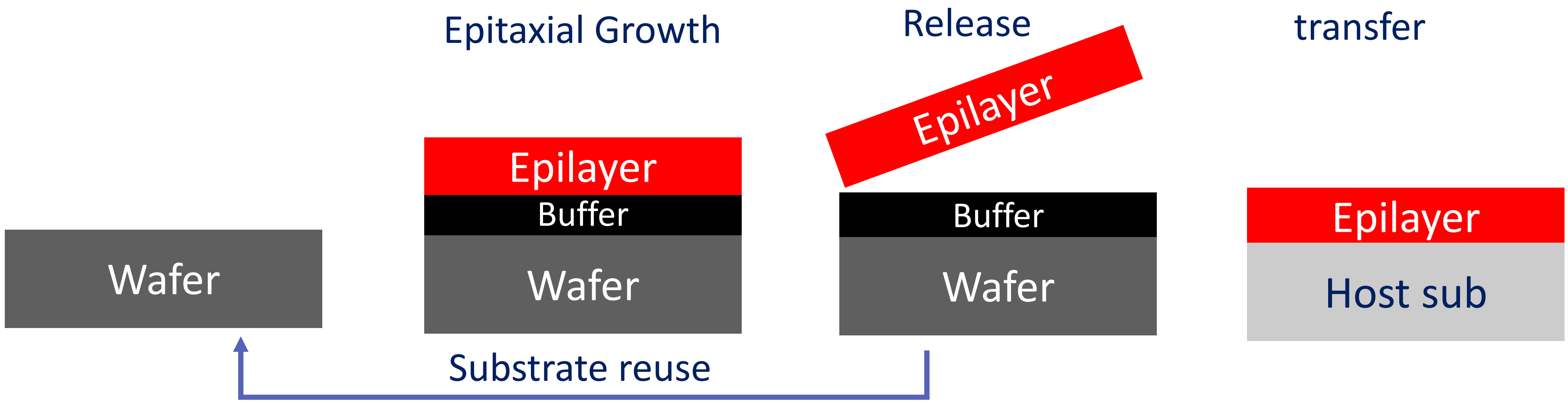
Price:
SiC > InP > GaAs > Ge >>> Si

Limited application

Lattice:
InP > GaAs/Ge > Si > SiC

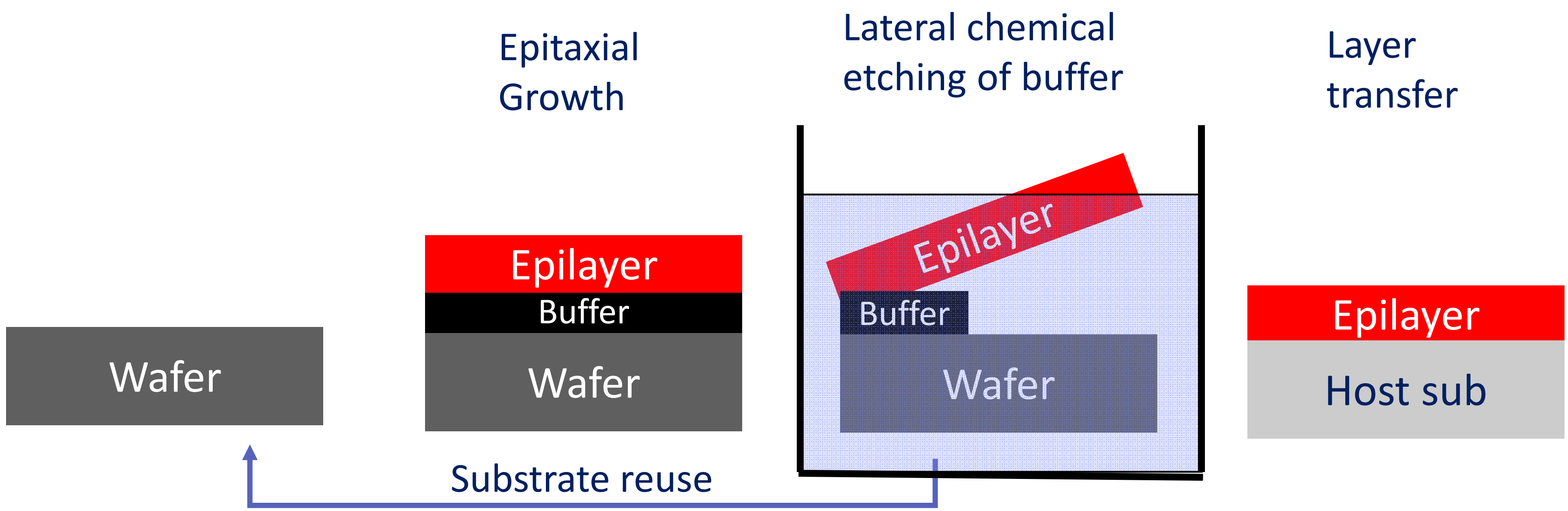
Defect generation

Layer transfer technology



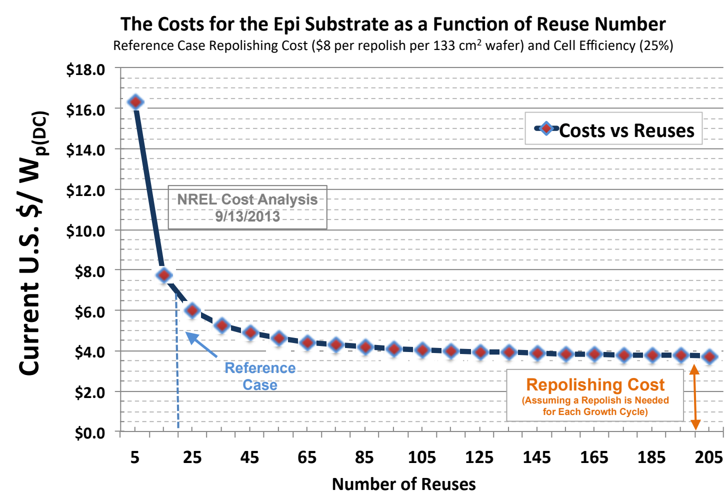
- **Requirements → Process cost must be cheaper than the substrate cost**
  - Wafer reusability
  - High throughput: Fast release
  - Minimum material consumption
    - Precise control of release interface
    - No post-release treatment (i.e. CMP)
  - Universality

Chemical lift-off (Epitaxial lift-off, ELO)



- **Pro: Control of release interface**
- **Cons:**
  - Post-treatment required
  - Slow release
  - Limited application mainly for GaAs & InP

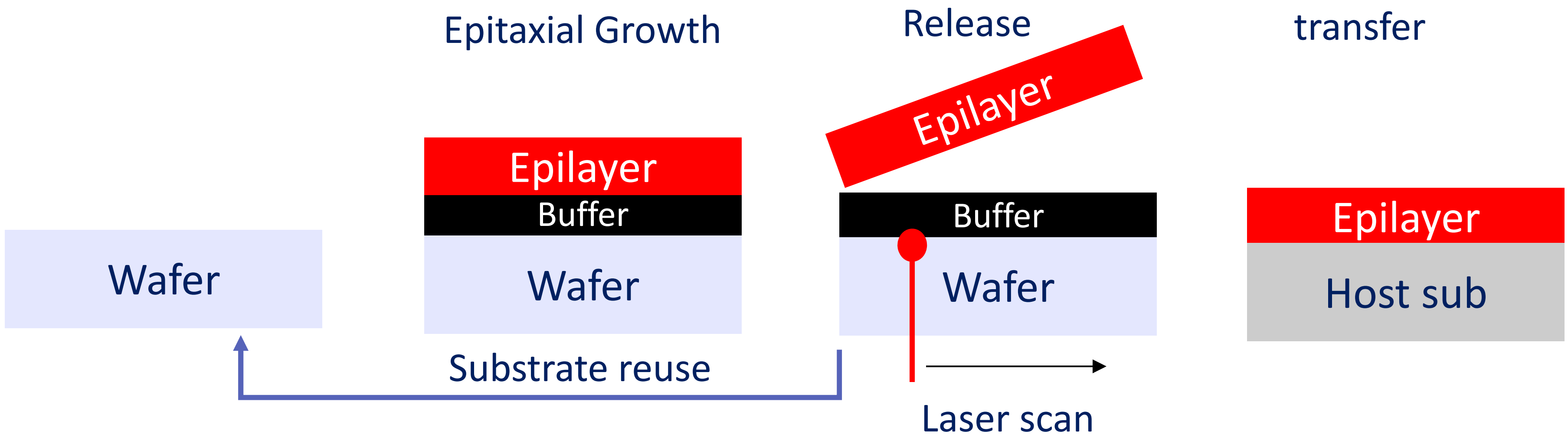
For PV applications



http://www.nrel.gov/docs/fy14osti/60126.pdf

E. Yablonovitch et al., *Appl. Phys. Lett.* 51, 2222 (1987). B. M. Kayes et al, *IEEE J. Photovolt.* 4, 729 (2014).

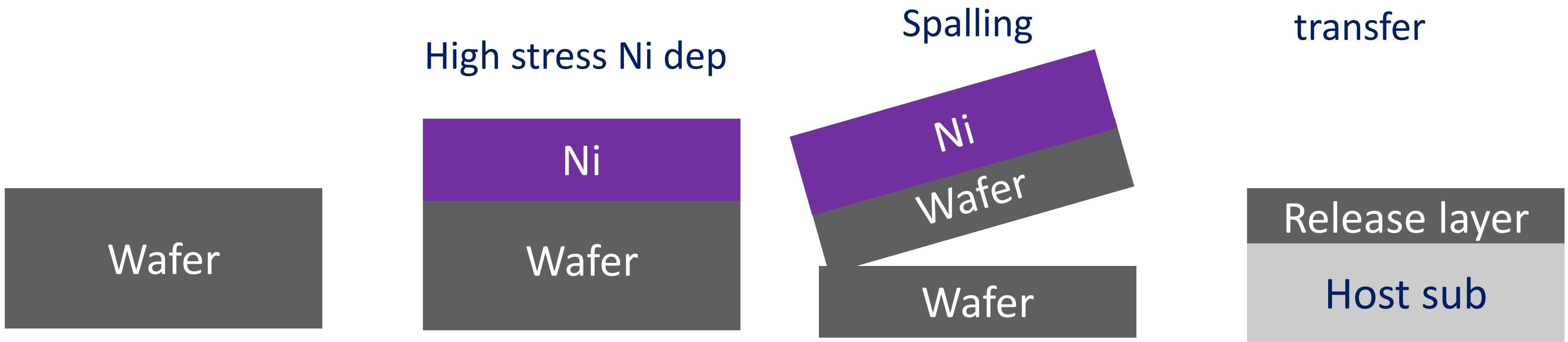
Optical lift-off (Laser lift-off, LLO)



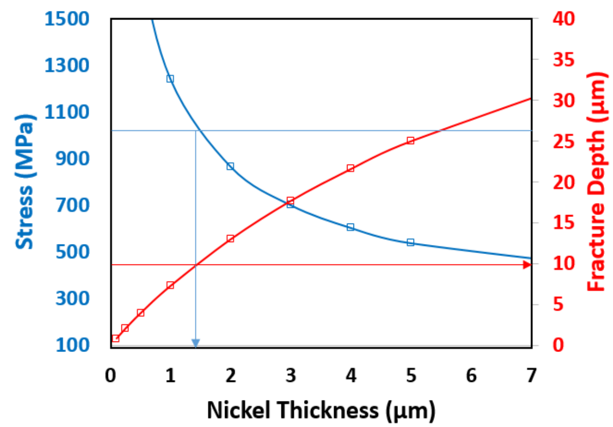
- **Pro: Control of release interface**
- **Cons:**
  - Post-treatment required
  - Cracking from local pressurization
  - Slow release
  - Limited application mainly for transparent substrate

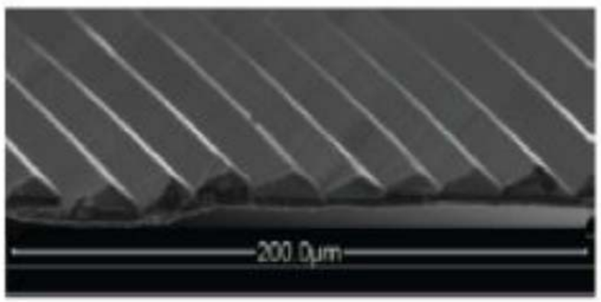
T. Ueda et al, Jap. J. of Appl. Phys. 50, 041001 (2011)
D. Iida et al., Appl. Phys. Lett. 105, 072101 (2014)
C.-Y. Lee. Appl. Phys. Exp. 7, 042103 (2014).

Mechanical lift-off (Spalling)



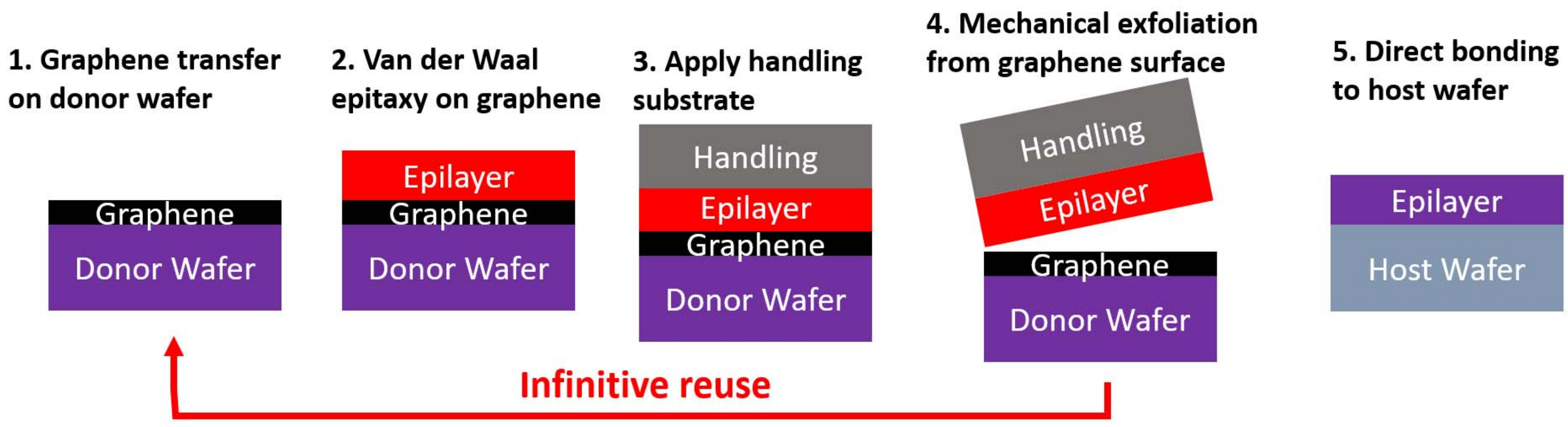
- **Pros:** Fast Release, Universally applied
- **Cons:**
  - Post-treatment required
  - Only applied for thick-layer release
  - Limited wafer reusability





Bedell et al., J. Phys. D: Appl. Phys. 46, 152002 (2013). Sweet et al., Photovoltaic Specialist Conference (2015)

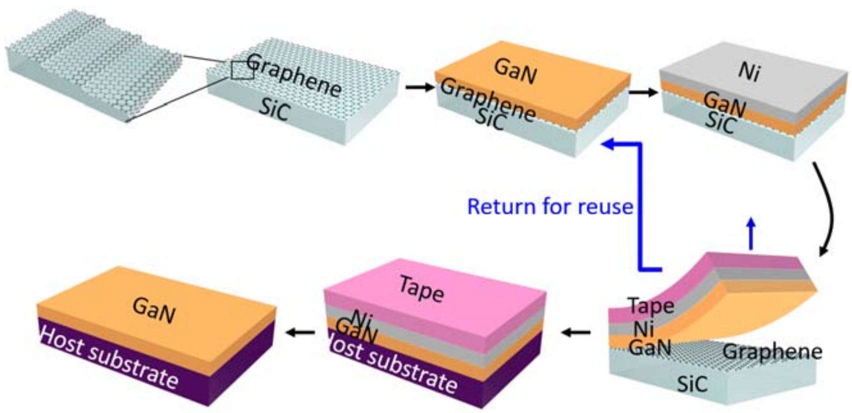
Graphene-based layer transfer (GBLT)

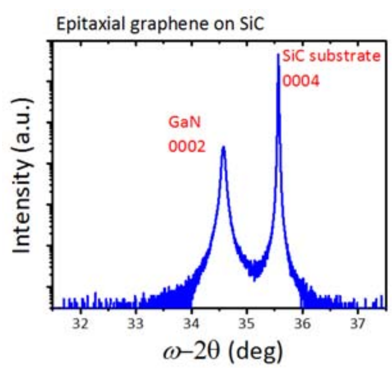


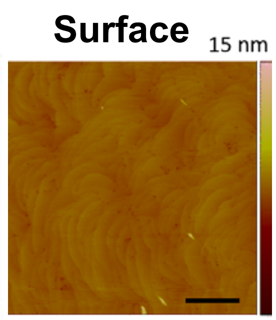
- **sp^2-bonded graphene: No broken bonds on the surface**
  - Precise release from graphene
  - Post-release treatment NOT required
  - **1 sec** release due to weak interaction
  - **Universal for any materials**

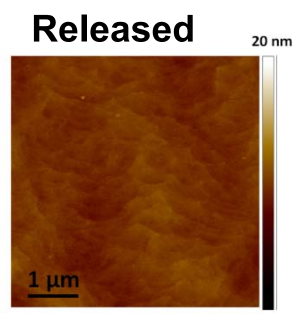
GaN on graphene

Growth/transfer Single-crystalline GaN on graphene





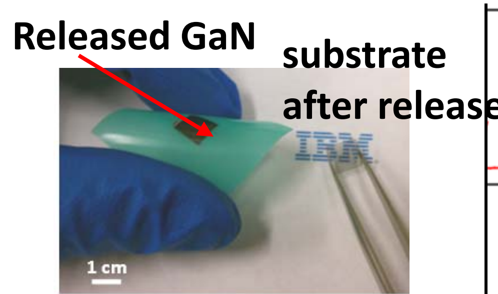


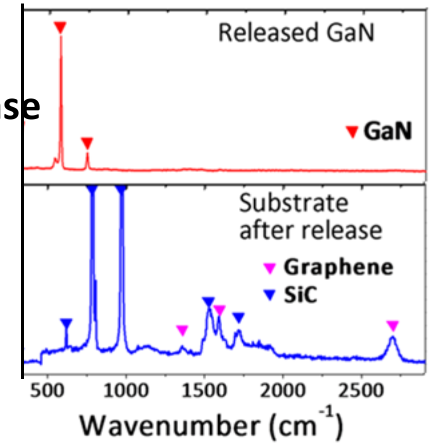


Direct growth without wetting layer

RMS roughness: 0.3 nm (surface), 0.5 nm (released)
Dislocation density: 9e8cm^{-2}
Single-crystallinity: Single-crystal

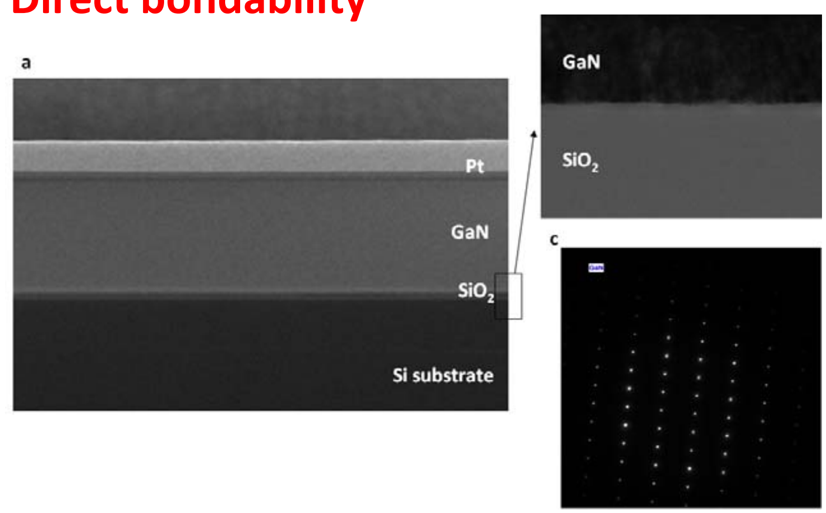
Substrate reusability





No post-treatment required for further recycle

Direct bondability

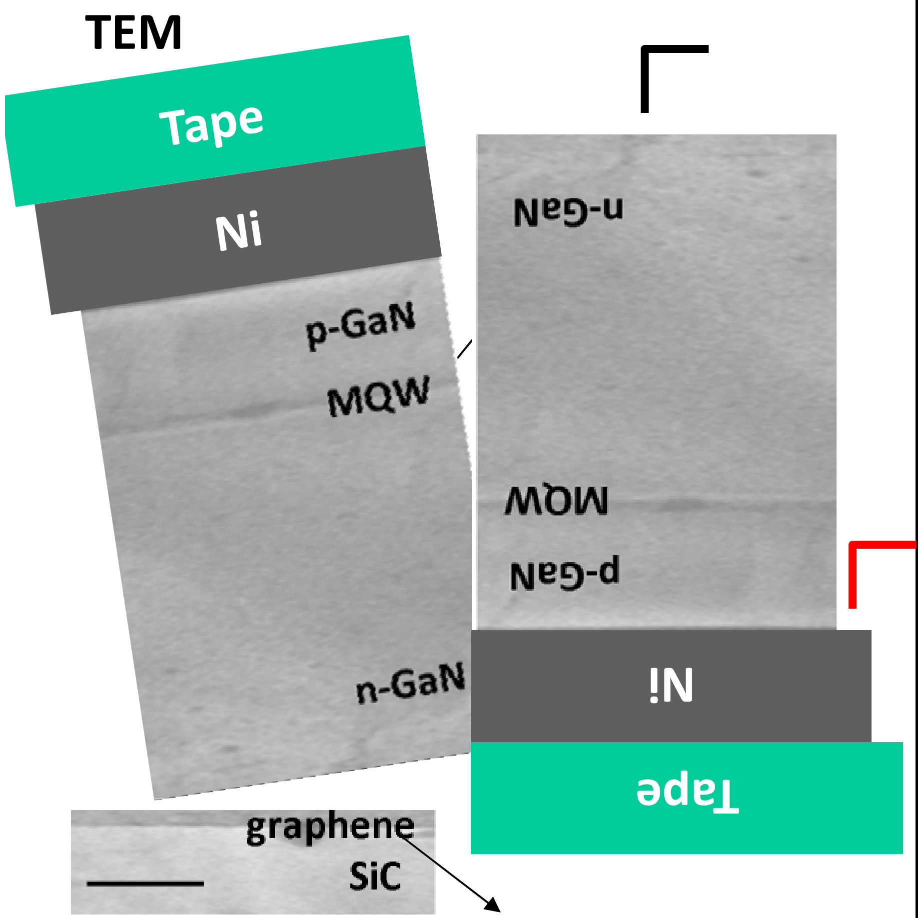


J. Kim et al., Nature Comm, Vol. 5, 4836 (2014)

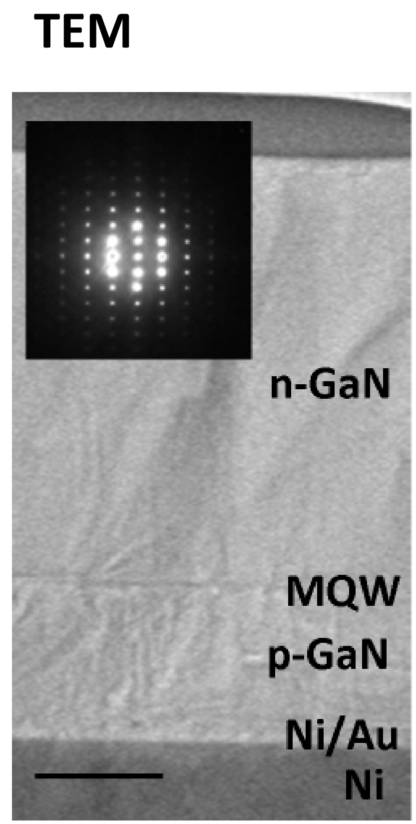
Graphene reusability

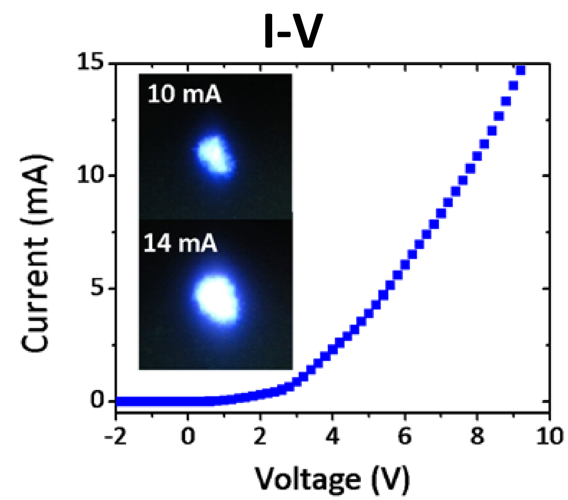
- **Blue LED growth on a recycled graphene/SiC substrate (3 times)**
  - Fabrication of GaN-based Blue LED on Tape by exfoliation

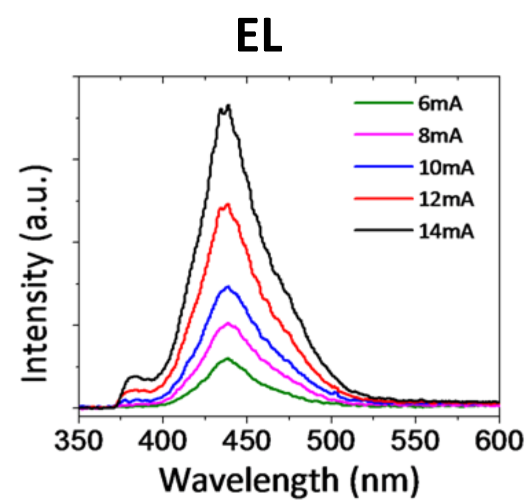
Before exfoliation



After exfoliation



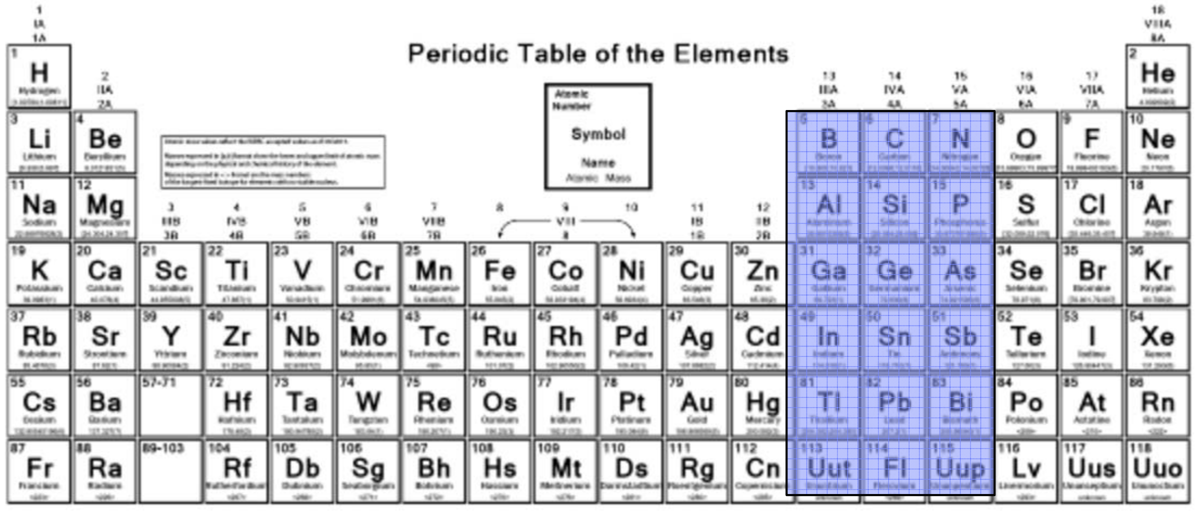


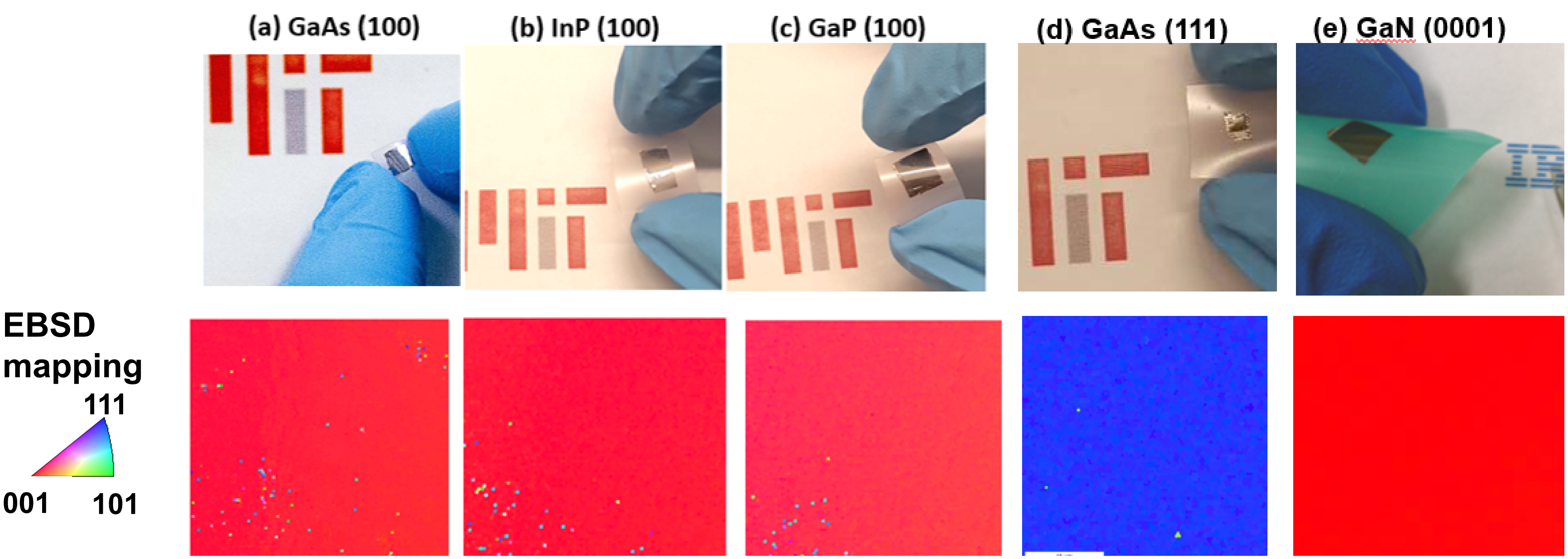


Jeehwan Kim *et al. Nature Communications*, Vol. 5, 4836 (2014)

Unversality of GBLT

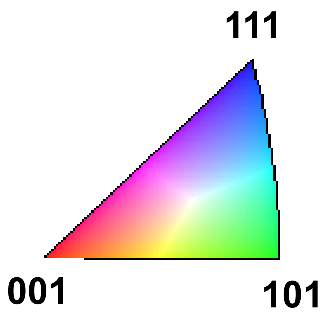
Growth of single-crystalline GaN, GaAs, InP, GaP, Ge on graphene

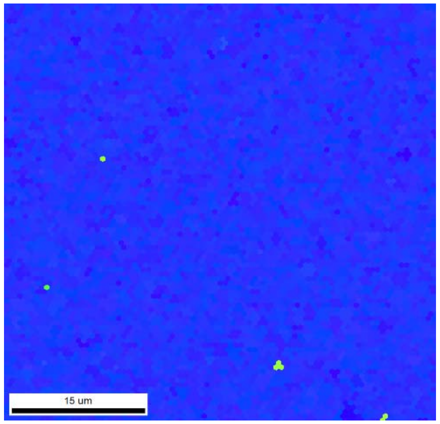




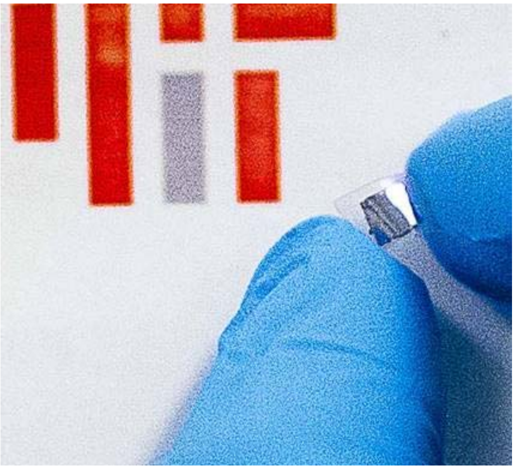
GBLT of GaAs

Single-crystalline GaAs grown on graphene

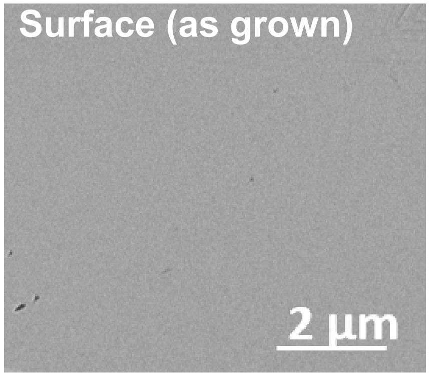


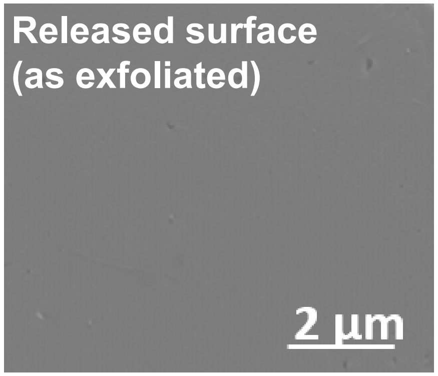


Successful exfoliation precisely from graphene

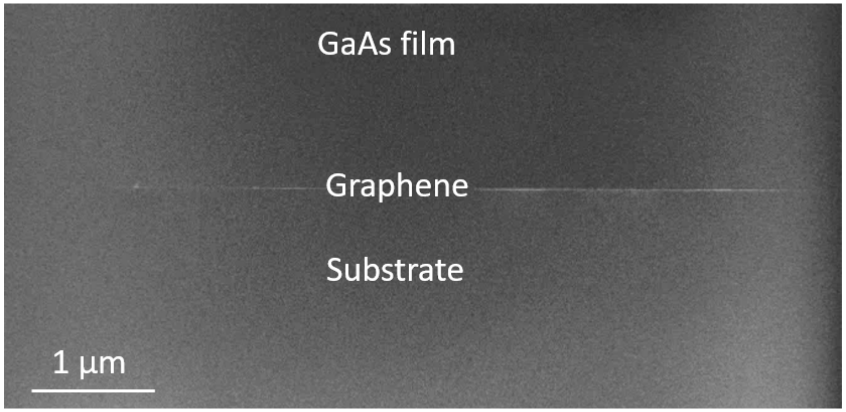


XSEM: Smooth surface morphology





Dark field XTEM: Strain field

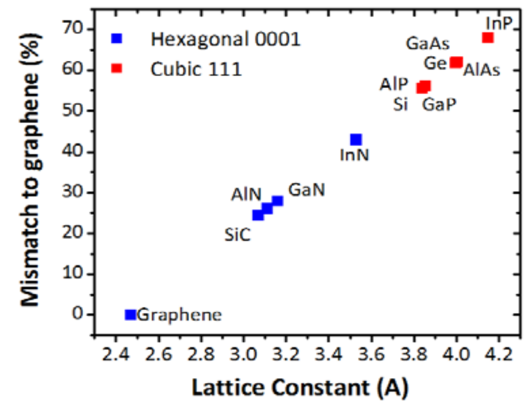


No sign of dislocation

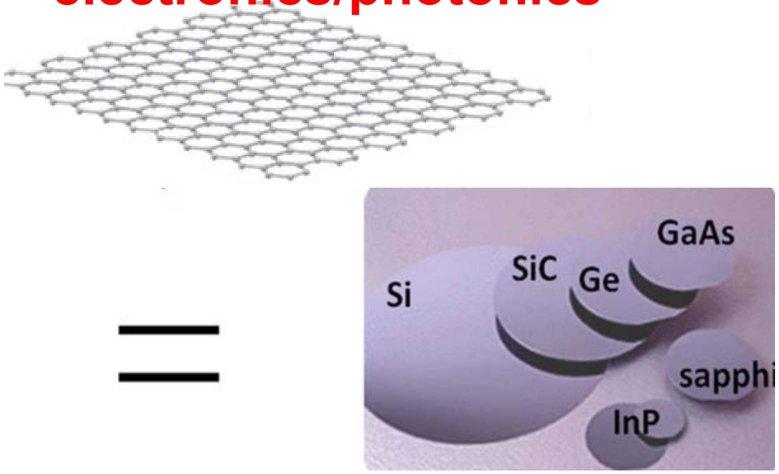
Y. Kim, S. Cruz, J. Kim et al., Manuscript submitted (2016)

Role of graphene

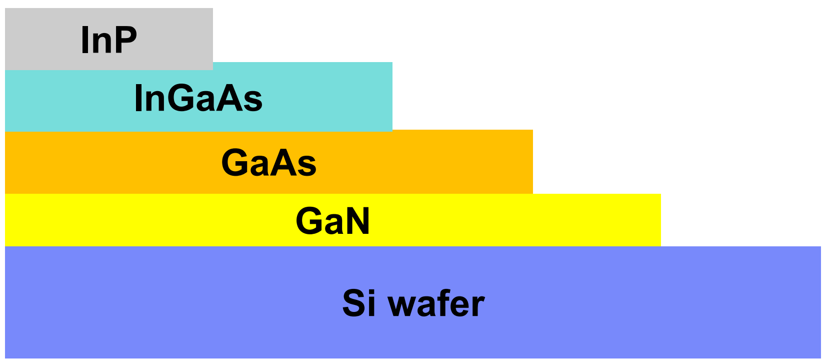
- Universal epitaxial seed layer → Growth of any semiconductors
- Dislocation-reducer/filter
- Release layer → 1sec release
- Wafer Surface protection → infinite reuse



Wide application of non-Si electronics/photonics

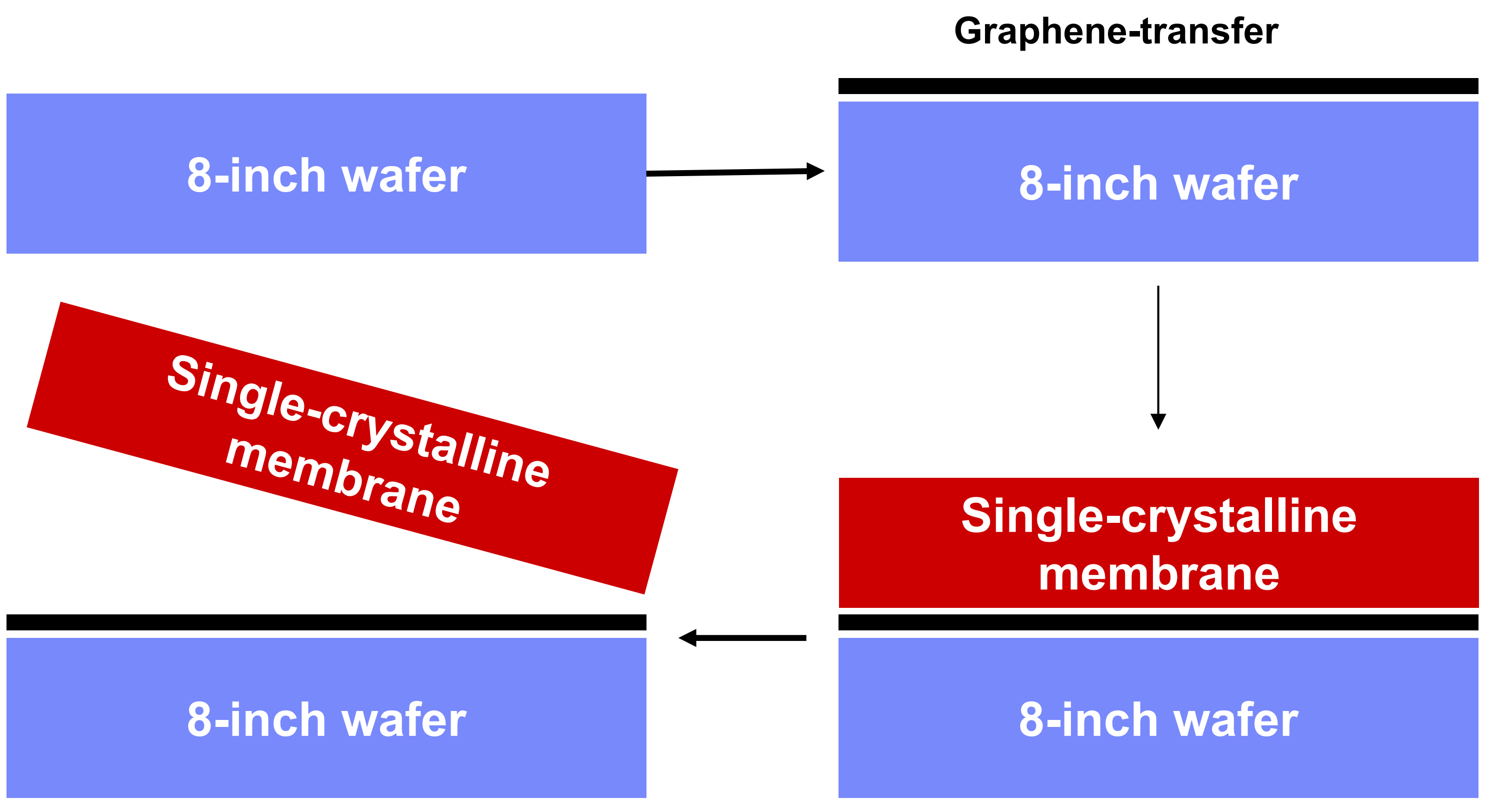


Enabled heterointegration



Application goals: Large-scale dislocation-free membrane

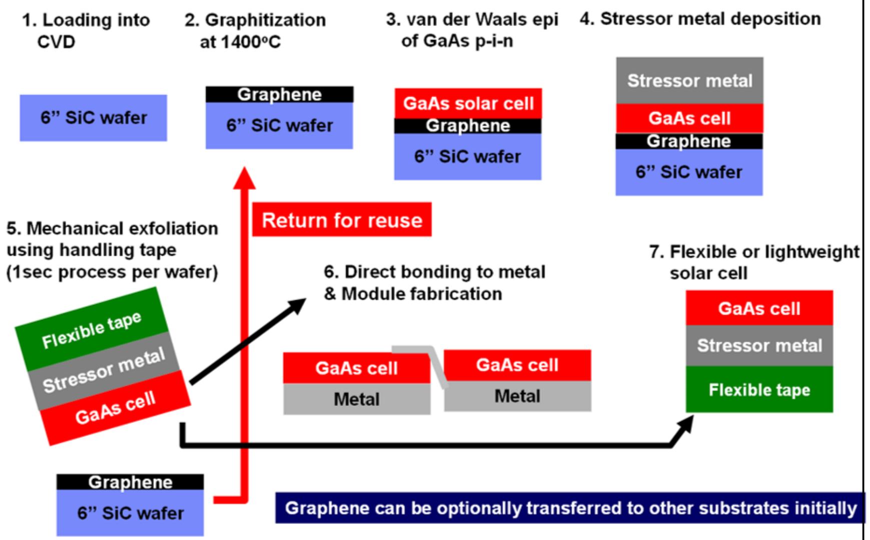
- 8-inch GaN, AlN, Diamond etc



Application: Cost-effective device manufacturing

- photovoltaics/LEDs/Powertransistors/heterointegration/3D IC

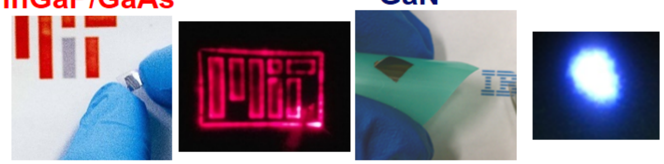
Advanced photovoltaics

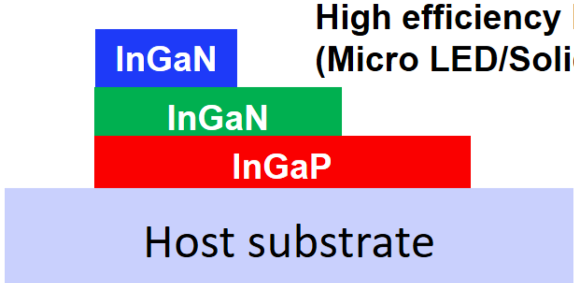


Advanced LEDs

InGaP/GaAs

GaN

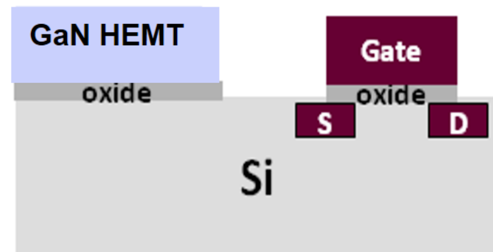




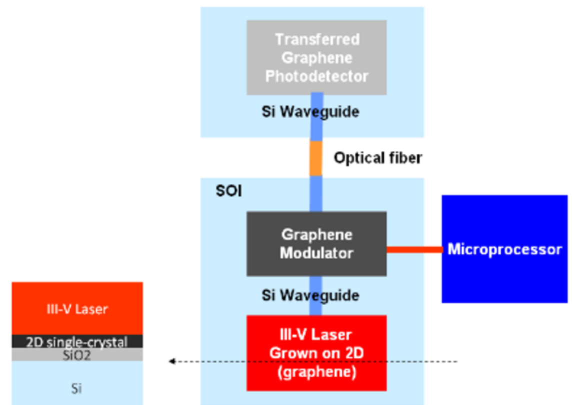
High efficiency RGB
(Micro LED/Solid state lighting)

Heterointegration

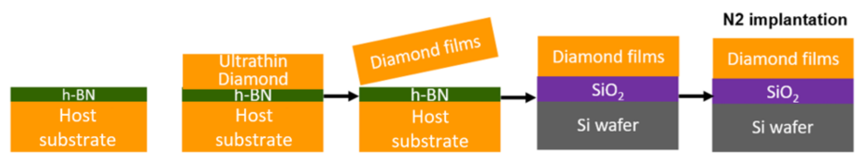
Power transistor



optical interconnect



Quantum computing



Highly uniform advanced RRAM

- Epitaxial RAM (ERAM)

Conventional Random Access Memory

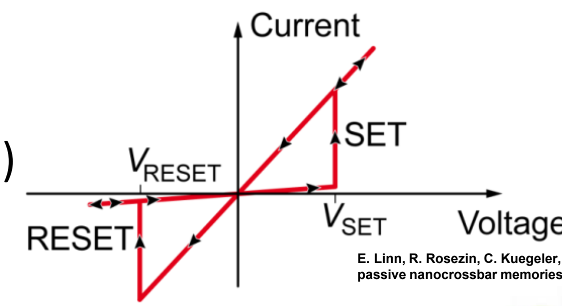
	DRAM	SRAM	Flash (NAND)	FeRAM	STT-MRAM	PCRAM	RRAM(ECM)	RRAM(VCM)
Structure	1T1C	6T	1T	1T1C	1(2)T1R	1T(D)1R	1R	1R
Cell Area	$6F^2$	$140F^2$	$4F^2$	$22F^2$	$20F^2$	$4F^2$	$4F^2$	$4F^2$
W/E Time	< 10 ns	0.2 ns	1/0.1 ms	65 ns	35 ns	100 ns	< 1 ns	< 1 ns
Retention Time	64 ms	N/A	10 y	10 y	> 10 y	> 10 y	1000hr at 200 °C	3000 hr at 150°C
Write Cycles	> 1E16	> 1E16	1E5	1E14	> 1E12	1E9	1E10	1E12
Write Operating Voltage (V)	2.5	1	15-20	1.3 - 3.3	1.8	3	0.6V	1-3V
Read Operating Voltage (V)	1.8	1	4.5	1.3 - 3.3	1.8	1.2	0.2V	0.1 - 0.2 V
Single Cell Write Energy (J/Bit)	4 fJ	0.5 fJ	0.4 fJ	30 fJ	2.5 pJ	6 pJ	1pJ (W), 8pJ (E)	115fJ(W), < 1pJ (E)

- ITRS 2013

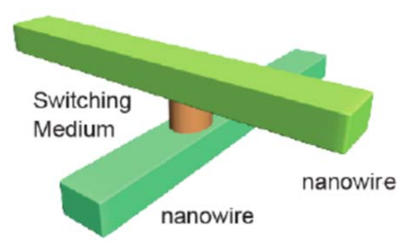
Why Resistive Random Access Memory (RRAM)?

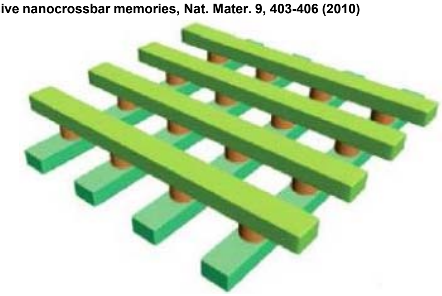
Devices based on resistive switching have been identified as a major contender in applications ranging from non-volatile memory storage, logic, to neuromorphic systems

- High scalability (10nm size)
- Endurance up to 10^{12}
- <ns switching
- Large connectivity (2-terminal structure)
- Long retention
- Low energy consumption
- 3D structure
- CMOS compatibility



E. Linn, R. Rosezin, C. Kuegeler, and R. Waser, Complementary resistive switches for passive nanocrossbar memories, Nat. Mater. 9, 403-406 (2010)





S. H. Jo, et al., *Nano lett.*, 9, 2009.

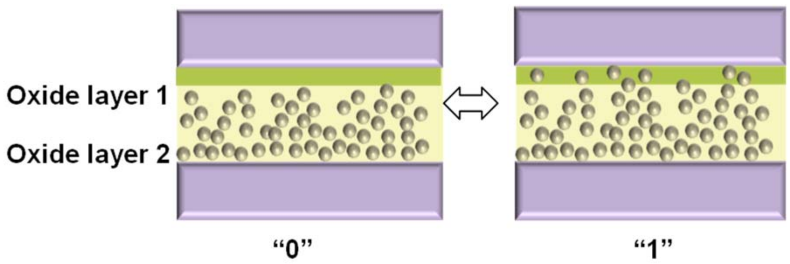
Required device functions for commercialization

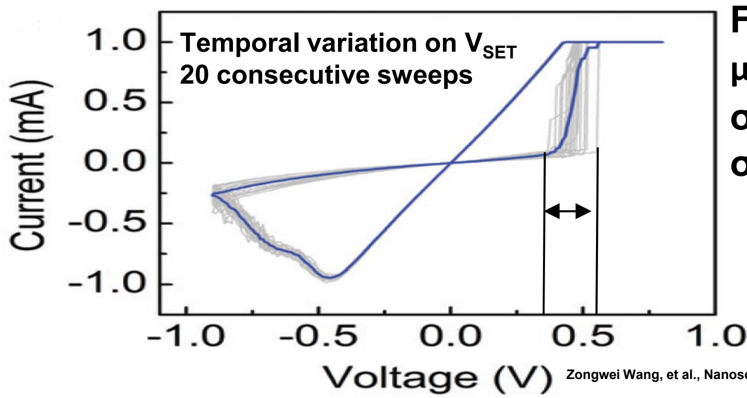
- ❑ Low energy consumption
- ❑ High endurance and high retention
- ❑ **High on-off ratio**
- ❑ **Cycle-to-cycle uniformity**
- ❑ **Device-to-device uniformity**
- ❑ **Current suppression in low voltage/reverse bias → Suppression of sneak paths**
- ❑ Parallelism for neuromorphic computing
- ❑ Multibit operation for neuromorphic computing

Currently developed ReRAMs do not support those functions

Conventional ReRAM devices- Valence Change Memory (VCM)

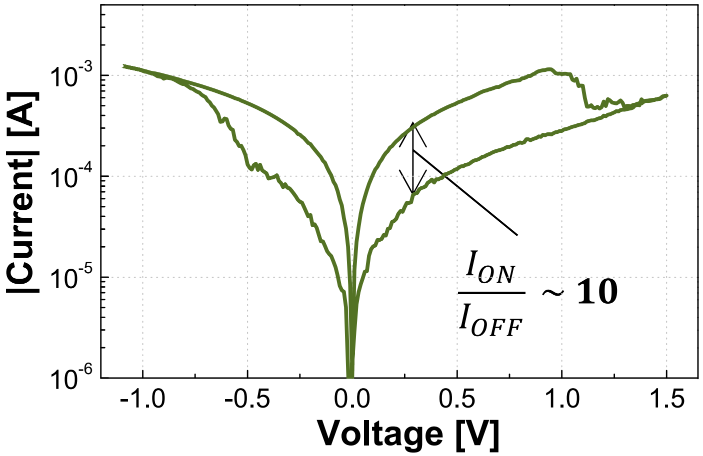
- **Good endurance and retention**
  - TaOx/Ta2O5 device :
    10^{12} write cycles with 10 years retention at 85°C
- **Device non-uniformity**
  (Cycle-to-cycle / Device-to-device)
  - Conductive filament is not confined in single path
    that cause stochastic uncorrelated switching events .
- **Low On-off ratio**
  - Digital: ~10 / Analog: ~2



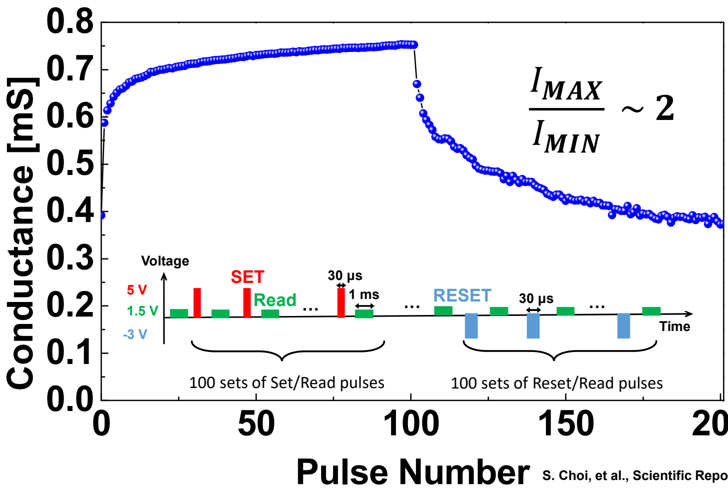


For V_{SET},
μ = 0.45 V
σ =0.05 V
σ/μ = 0.11

Zongwei Wang, et al., Nanoscale, 8, 14015-14022 (2016)

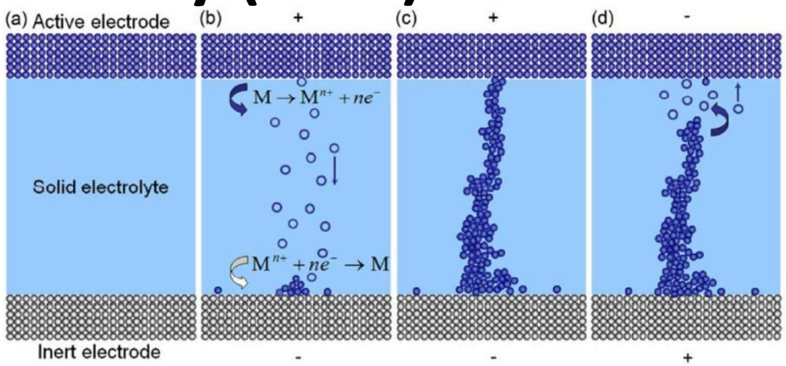


S. Kim, et al., ACS Nano, 8, 10262-10269 (2014)

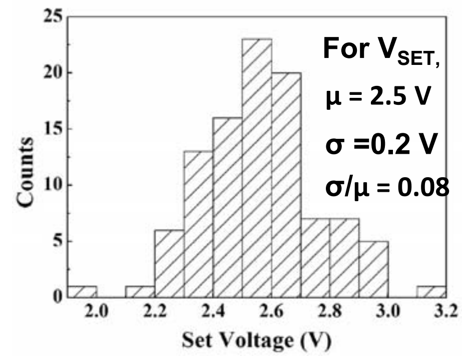


S. Choi, et al., Scientific Reports, 5, (2015)

Conventional ReRAM devices- Electrochemical Metallization Memory (ECM)

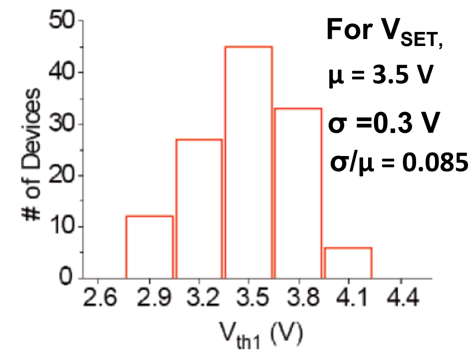


Cycle-to-cycle variation



S. Gaba, et al., IEEE EDL, 35, 2014

Device-to-device variation



S.H. Jo, et al., Nano Lett., 8, 2008

- **High On-off ratio**
  - Digital > 10^4 For reduced power, reduced bit-error-rate(BER) and increased read bandwidth in high density RRAM
- **Device non-uniformity**

  (Cycle-to-cycle / Device-to-device)
- **Retention/Endurance trade-off**
  - Weak Ag-channel formation enhances endurance but reduces retention time
  - Strong Ag-channel formation increases retention time but deteriorate endurance

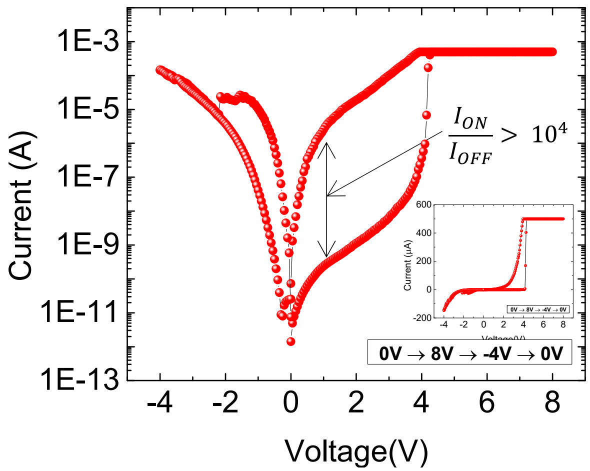
New epitaxial RAM (ERAM) devices
(invented by Kim group at MIT)

- **Long retention with long endurance**
- **Excellent device uniformity**
- **High on/off ratio**
  - good for both analog and digital
    - Analog: >500, Digital: 10^4
- **Current suppression in low voltage to reduce the impact of sneak path**

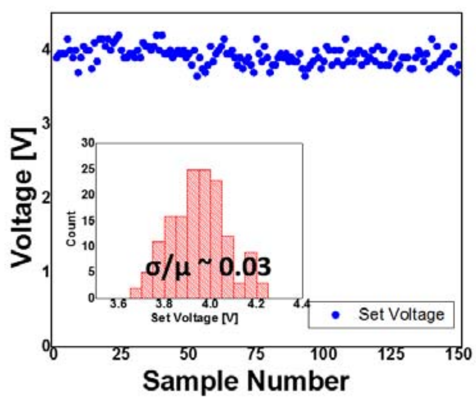
This will enable large-scale memory arrays for digital application as well as for neuromorphic computing

Digital switching behavior/uniformity of ERAM

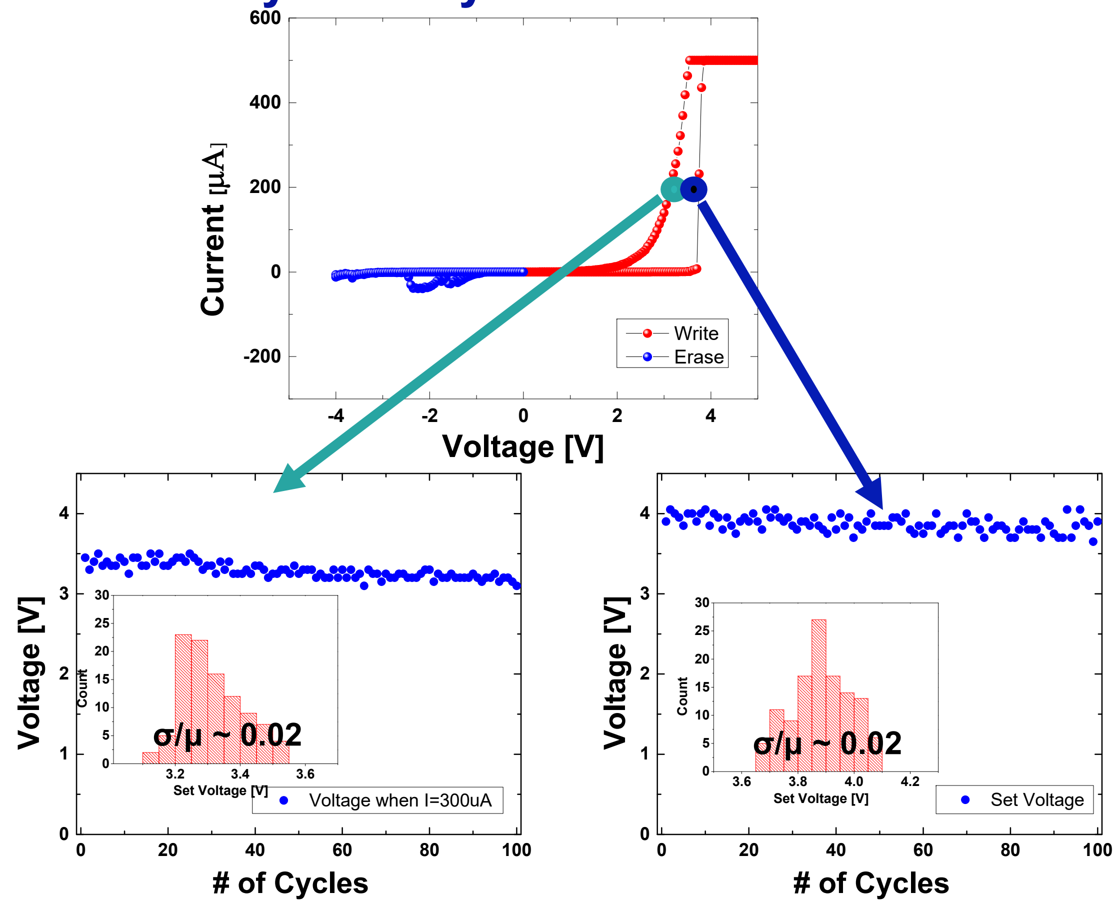
DC sweep



Device-to-device variation



Cycle-to-cycle variation

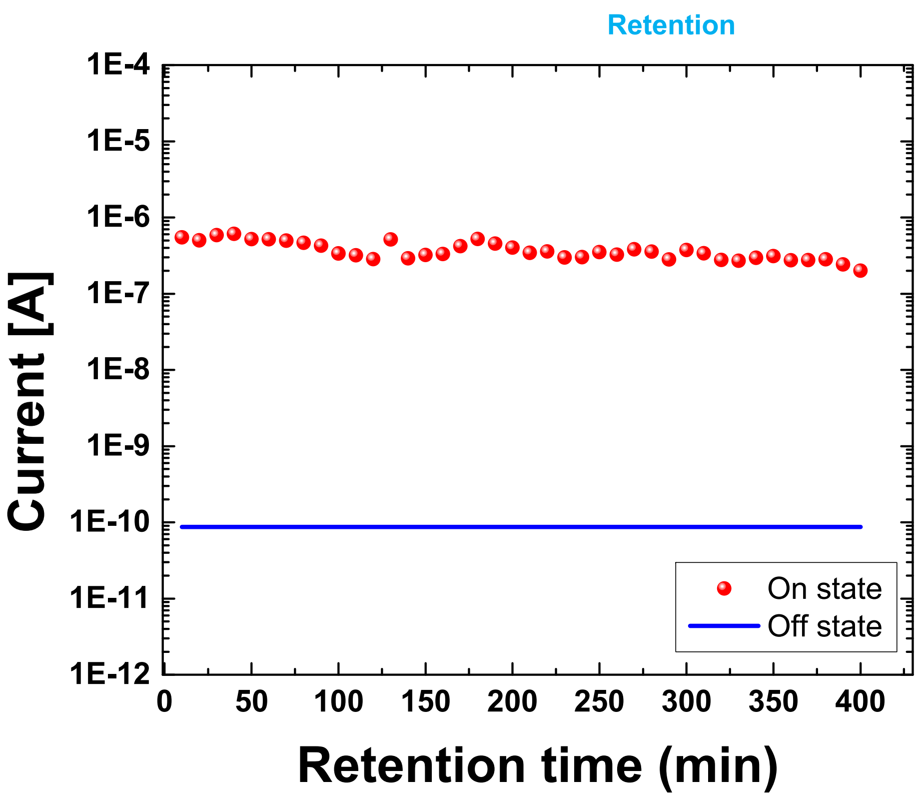


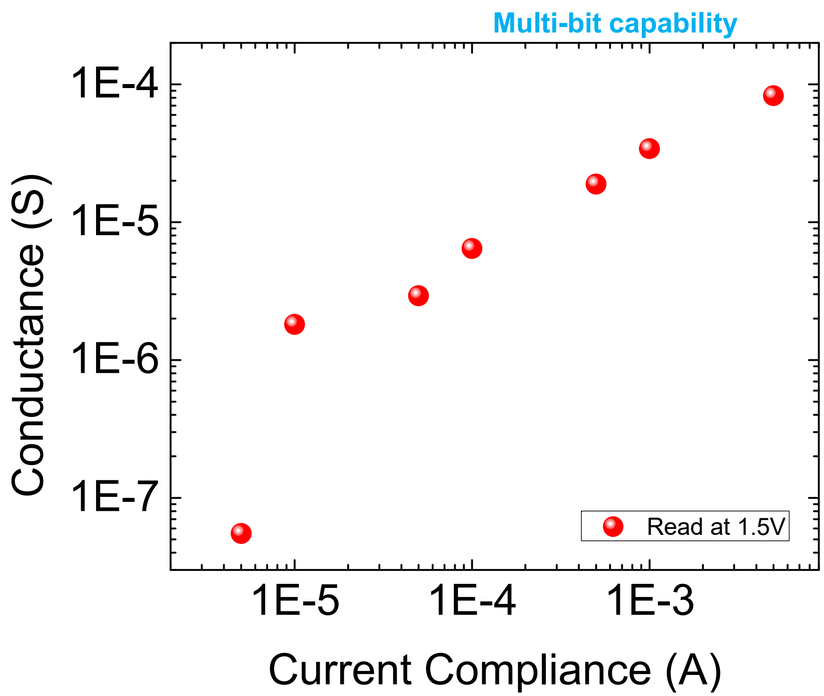
Voltage distribution at on-state

Set voltage distribution

1. High On/Off ratio > 10^4
2. Excellent cycle-to-cycle and device-to-device uniformity
3. Suppression of low current (reduction of sneak path in arrays)

Digital application

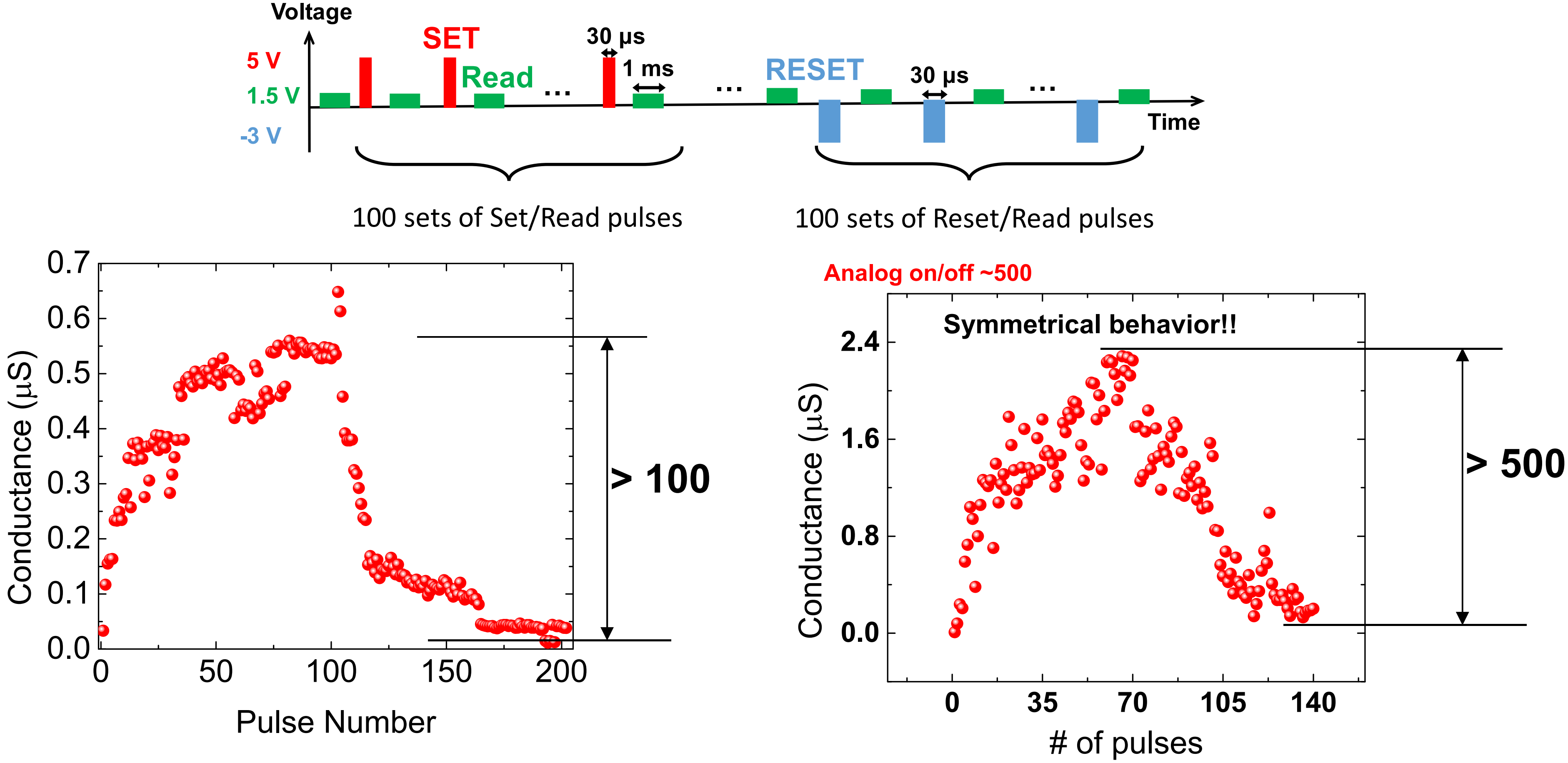




> 8 hours retention test
No current reduction observed.

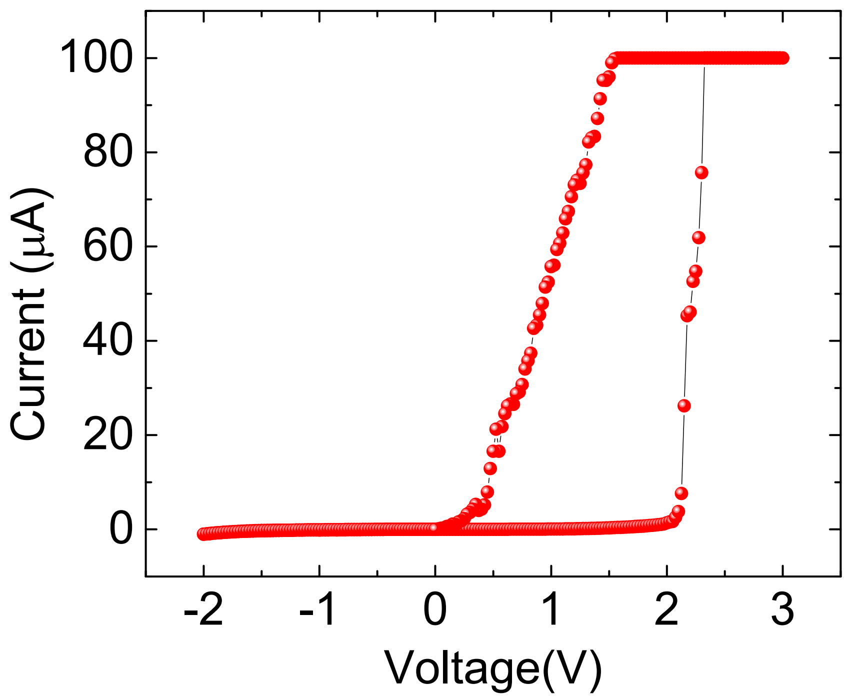
Multilevel storage from self-limiting filament growth by current-compliance

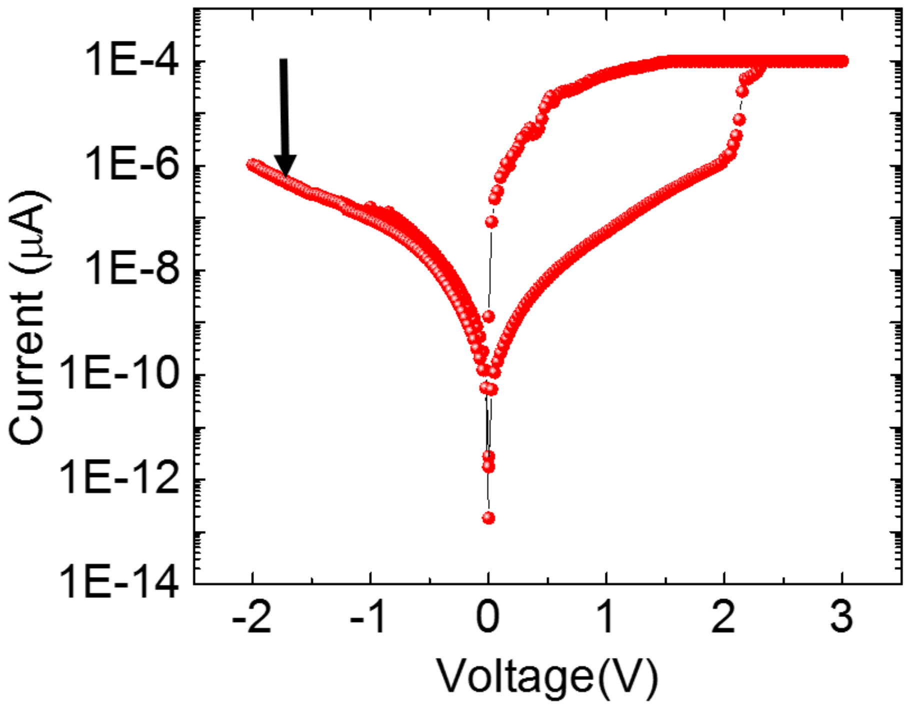
Analog switching behavior of ERAM



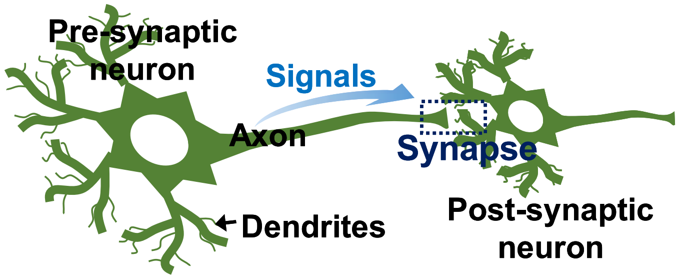
- **The analog switching behavior offers an effectively implement synaptic functions**
- **The devices show large dynamic ranges with easier access to the intermediate states that are suitable for neuromorphic computing applications**

Self-selection behavior of ERAM



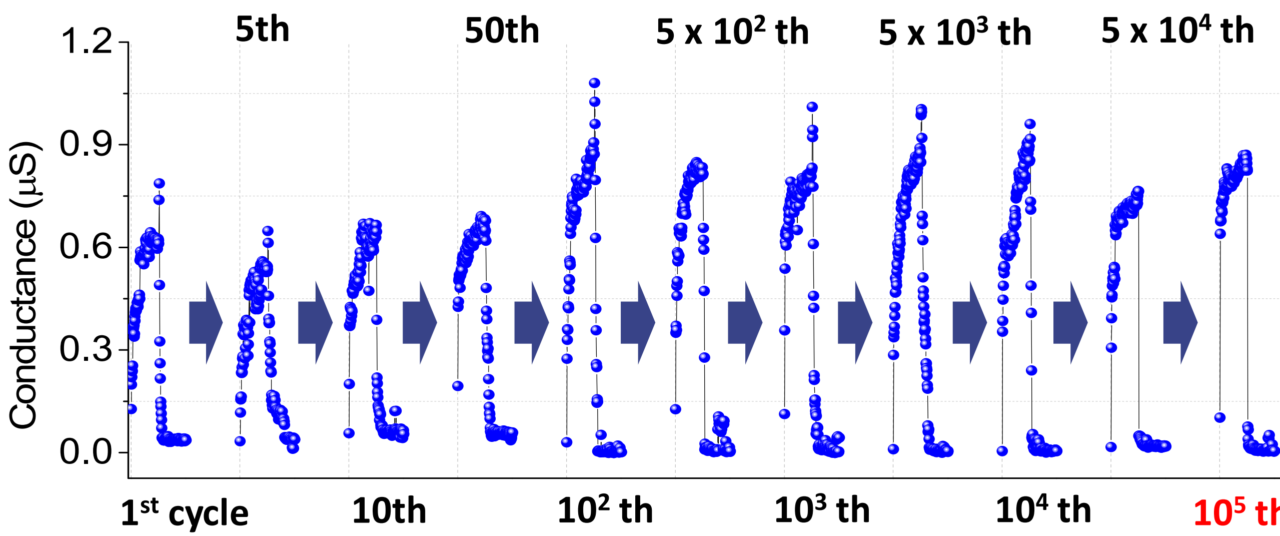


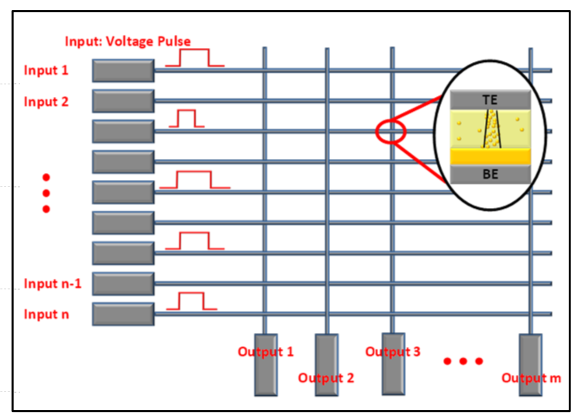
Neuromorphic application



S. H. Jo, et al., *Nano lett.*, 9, 2009.

- **The analog switching behavior an effectively implement synaptic functions and enable efficient neuromorphic systems.**
- **High On/Off current ratio with long retention and endurance**
  - Suitable for large-array neuromorphic computing and demonstration of basic synaptic learning rules such as spike-timing-dependent plasticity (STDP)





Properties of ERAM

1. Good endurance and retention
2. Highly uniform devices
   - Device yield=100%, No variation in device-to-device/cycle-to-cycle
3. High on-off ratio: digital >10,000 / Analog 500
4. Self-selecting behavior
   → No need for selectors (=another source of non-uniformity)

Self-selecting

	Retention	Endurance	Retention & Endurance	On-off ratio	Uniformity
VCM	Excellent	Excellent	Excellent	Low	Good
ECM	Excellent	Excellent	Bad	High	Bad
OURS	**Excellent**	**Excellent**	**Excellent**	**High**	**Excellent**

OUR GOALS

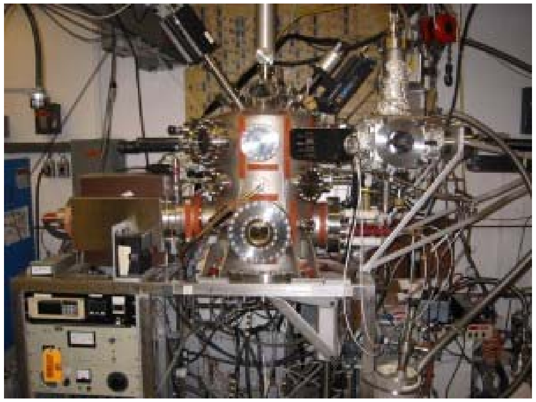
1. Fabricating extremely large-scale arrays
2. Demonstration of synaptic learning rules such as spike-timing-dependent plasticity
3. First demonstration of cognitive computing with ReRAM

Equipment

8" two-chamber MBE system (III-N and III-V)

4" UHV CVD (epitaxial graphene, SiC, Si, Ge, diamond)

2" MBE system (II-VI)



6" MOCVD (III-V, Si, Ge)

Collaborators

MIT:
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Harvard: Philip Kim

OSU: Jinwoo Hwang

UIUC: Minjoo Larry Lee

IBM: Tze-Chiang Chen, Frances Ross, James Hannon, Devendra Sadana

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Yunjo Kim (Nano)

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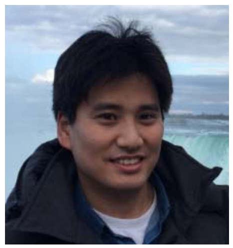
Kuan Qiao (Physics)

Postdocs

Dr. Shinhyun Choi (EE)



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